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NEW SCHEME

Third Semester B.E. Degree Examination, July 2007
CS / IS / EE / EC / IT / TC / BM / ML
Logic Design

Time: 3 hrs. [Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Using the theorems of Boolean algebra, simplify the following:

i) $y_1 = D(\overline{A} + B) + \overline{B}(C + AD)$

ii) $y_2 = \overline{\overline{A\overline{B} + ABC + A(B + A\overline{B})}}$

iii) $y_3 = \overline{AB\overline{C}} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$ **(09 Marks)**

b. Express the following expressions in canonical form:

i) $y_1 = (A - B)(A + C)(B + \overline{C})$

ii) $y_2 = AC + AB + BC$ **(06 Marks)**

c. Give the implementation of EXOR gate using minimum number of NAND gates only. **(05 Marks)**

2 a. i) Express the following min term expression in POS form:
$y(A, B, C, D) = \Sigma m(1, 3, 5, 6, 7, 9, 10, 12, 15)$

ii) Express the following max term expression in SOP form:
$y(A, B, C) = \pi M(0, 3, 5, 6)$. **(06 Marks)**

b. i) What are the advantage, disadvantages of K map?

ii) Simplify the following function in SOP form using K Map:
$f(A, B, C, D) = \overline{A}\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C}$ **(08 Marks)**

c. Simplify the following function in POS form using K map:
$f(A, B, C, D) = \pi M(0, 1, 2, 5, 8, 9, 10)$. **(03 Marks)**

d. Simplify the following function in SOP form using K map:
$y(w, x, y, z) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(03 Marks)**

3 a. Minimize the expression using Quine Mc Cluskey method.
$y(A, B, C, D) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(10 Marks)**

b. Simplify the following using VEM technique. Reduce 4 variables to 3 variables.
$y = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}BC\overline{D} + ABCD + AB\overline{C}\overline{D}$ **(05 Marks)**

c. Realize a full adder using minimum number of 2 input NAND gates. Write the truth table, relevant expressions and logic diagram. **(05 Marks)**

4 a. Define the following:
i) Fan in and fan out
ii) Noise margin
iii) Propagation delay. **(06 Marks)**

b. Explain the operation of basic TTL NAND gate circuit with relevant diagram. **(07 Marks)**

c. Draw and explain the circuit of 2 input CMOS NOR gate. **(07 Marks)**

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5 a. What is a magnitude comparator? Design a 2 bit digital comparator by writing the truth table, the relevant expression, and logic diagram. **(10 Marks)**

b. Implement the following Boolean function using 8:1 MUX:
$F(A, B, C, D) = \Sigma m(1, 2, 5, 9, 10, 14)$ **(06 Marks)**

c. Write the truth table of the following flip flops:
D, T, SR, JK. **(04 Marks)**

6 a. Write the excitation table of SR flip flop. Design a synchronous MOD-6 counter using SR flip flop for the following count sequence 0, 1, 3, 2, 6, 4 and repeat. Write the transition table, logic diagram. **(10 Marks)**

b. What is a look-ahead carry adder? Explain the circuit and operation of a 4 bit binary adder with look-ahead carry. **(10 Marks)**

7 a. Realize a 3 bit binary synchronous up counter using JK flip flop. Write the excitation table, transition table and logic diagram. Include preset, clear option. **(10 Marks)**

b. Explain the different types of shift register. SISO, SIPO, PIPO, PISO with relevant circuit diagram. **(10 Marks)**

8 a. A combinational circuit is defined by the functions:
$F_1 = \Sigma m(3, 5, 7)$
$F_2 = \Sigma m(4, 5, 7)$
Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 outputs. **(08 Marks)**

b. A sequential network has one input and one output. The state diagram is shown in fig.8(b). Design the sequential circuit with T flip flop. **(12 Marks)**

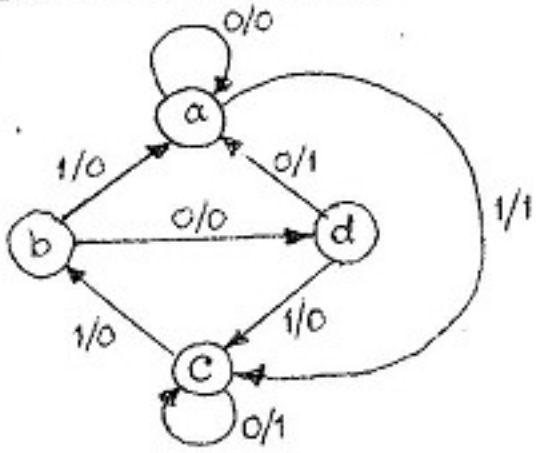

Fig.8(b)